WHAT IS CLAIMED IS:

1. An apparatus for converting an analog signal to a digital signal, the apparatus comprising:

a plurality of capacitors including at least a first capacitor, a second capacitor and a third capacitor, a first capacitor associated with a first capacitance, a second capacitor associated with a second capacitance, a third capacitor associated with a third capacitance, the first capacitance being substantially equal to the second capacitance, the second capacitance being substantially equal to the third capacitance;

a plurality of resistors including at least a first resistor and a second resistor, the first resistor associated with a first resistance, a second resistor associated with a second resistance, the first resistance being substantially equal to the second resistance;

an operational amplifier including at least a first input terminal, a second input terminal and an output terminal;

wherein the first capacitor includes a first capacitor terminal and a second capacitor terminal, the second capacitor includes a third capacitor terminal and a fourth capacitor terminal, the third capacitor includes a fifth capacitor terminal and a sixth capacitor terminal, and the first capacitor terminal, the third capacitor terminal, and the fifth capacitor terminal are coupled to the first input terminal;

wherein the second input terminal is coupled to a first voltage;

wherein each of the second capacitor terminal, the fourth capacitor terminal, and the sixth capacitor terminal is capable of being coupled to anyone of the first voltage, an analog voltage, a second voltage, and a third voltage, the analog voltage associated with the analog signal;

wherein the first resistor includes a first resistor terminal and a second resistor terminal, the second resistor includes a third resistor terminal and a fourth resistor terminal, the first resistor terminal is coupled to the second voltage, the fourth resistor terminal is coupled to the first voltage, the first resistor and the second resistor being in series;

wherein the third voltage is capable of being coupled to anyone of at least the first resistor terminal, the second resistor terminal, and the third resistor terminal;

wherein the apparatus is configured to convert the analog signal to the digital signal and is associated with a process related to a successive approximation register;

wherein the process includes processing information associated with the analog voltage and a fourth voltage; adjusting the fourth voltage in response to information associated with the analog voltage and the fourth voltage, and determining the digital signal based on at least information associated with the fourth voltage;

wherein the fourth voltage is associated with at least a first voltage level of the second capacitor terminal, a second voltage level of the fourth capacitor terminal and a third voltage level of the sixth capacitor terminal, the first voltage level, the second voltage level and the third voltage level each being selected from a group consisting of the first voltage, the second voltage and the third voltage.

2. The apparatus of claim 1 wherein the first voltage is at the ground level.

3. An apparatus for converting an analog signal to a digital signal, the apparatus comprising:

a plurality of capacitors including at least a first capacitor and a second capacitor, a first capacitor associated with a first capacitance, a second capacitor associated with a second capacitance, the first capacitance being substantially equal to the second capacitance;

a plurality of resistors including at least a first resistor and a second resistor, the first resistor associated with a first resistance, a second resistor associated with a second resistance, the first resistance being substantially equal to the second resistance;

an operational amplifier including at least a first input terminal, a second input terminal and an output terminal;

wherein the first capacitor includes a first capacitor terminal and a second capacitor terminal, the second capacitor includes a third capacitor terminal and a fourth capacitor terminal, and the first capacitor terminal and the third capacitor terminal are coupled to the first input terminal;

wherein the second input terminal is coupled to a first voltage;

wherein each of the second capacitor terminal and the fourth capacitor terminal is capable of being coupled to anyone of the first voltage, an analog voltage, a second voltage, and a third voltage, the analog voltage associated with the analog signal;

wherein the first resistor includes a first resistor terminal and a second resistor terminal, the second resistor includes a third resistor terminal and a fourth resistor terminal, the

first resistor terminal is coupled to the second voltage, the fourth resistor terminal is coupled to the first voltage, the first resistor and the second resistor being in series;

wherein the third voltage is capable of being coupled to anyone of at least the first resistor terminal, the second resistor terminal, and the third resistor terminal;

wherein the apparatus is configured to convert the analog signal to the digital signal and is associated with a process related to a successive approximation register;

wherein the process includes coupling the second capacitor terminal and the fourth capacitor terminal to the analog voltage, processing information associated with the analog voltage and a fourth voltage, adjusting the fourth voltage in response to information associated with the analog voltage and the fourth voltage, and determining the digital signal based on at least information associated with the fourth voltage;

wherein the fourth voltage is associated with at least a first voltage level of the second capacitor terminal and a second voltage level of the fourth capacitor terminal; the first voltage level and the second voltage level each being selected from a group consisting of the first voltage, the second voltage and the third voltage.

4. The apparatus of claim 3 wherein the first voltage is at the ground level.

5. The apparatus of claim 3 wherein the plurality of capacitors is associated with a plurality of capacitances, each of the plurality of capacitances being substantially the same.

6. The apparatus of claim 5 wherein the plurality of capacitors is associated with a plurality of capacitor terminals, each of the plurality of capacitor terminals is capable of being coupled to anyone of the first voltage, the analog voltage, the second voltage, and the third voltage.

7. The apparatus of claim 6 wherein the plurality of capacitor terminals is free from the first capacitor terminal and the third capacitor terminal.

8. The apparatus of claim 7 wherein each of the plurality of capacitor terminals is coupled to the third voltage.

9. The apparatus of claim 7 wherein the plurality of resistors is associated with a plurality of resistances, each of the plurality of resistances being substantially the same.

10. The apparatus of claim 9 wherein the plurality of resistors are in series.

11. The apparatus of claim 10 wherein the plurality of resistors is associated with a plurality of voltages, the plurality of voltages including the second voltage and the first voltage, the plurality of voltages associated with a connection between any two of the plurality of resistors.

12. The apparatus of claim 11 wherein the third voltage is capable of being coupled to anyone of the plurality of voltages.

13. A method for converting an analog signal to a digital signal, the method comprising:

providing an apparatus for converting the analog signal to the digital signal, the apparatus including:

a plurality of capacitors associated with a plurality of capacitances, each of the plurality of capacitances being substantially equal;

a plurality of resistors in series and associated with a plurality of resistances, each of the plurality of resistances being substantially equal;

wherein the plurality of capacitors is associated with a first plurality of capacitor terminals and a second plurality of capacitor terminals, the first plurality of capacitor terminals is coupled to each other, each of the second plurality of capacitor terminals is capable of being coupled to anyone of a first voltage, an analog voltage, a second voltage, and a third voltage, the analog voltage associated with the analog signal;

wherein the plurality of resistors is associated with a plurality of resistor terminals, a first terminal of the plurality of resistor terminals is coupled to the second voltage, a second terminal of the plurality of resistor terminals is coupled to the first voltage;

wherein the third voltage is capable of being coupled to at least anyone of the plurality of resistor terminals free from the second terminal;

coupling each of the second plurality of capacitor terminals to the analog voltage;

decoupling each of the second plurality of capacitor terminals from the analog voltage;

coupling each of the second plurality of capacitor terminals to one selected from a group consisting of the first voltage, the second voltage, and the third voltage, the second plurality of capacitor terminals associated with a plurality of capacitor voltage levels respectively;

processing information associated with the analog voltage and a fourth voltage, the fourth voltage associated with the plurality of capacitor voltage levels;

adjusting the fourth voltage in response to information associated with the analog voltage and the fourth voltage;

determining the digital signal based on at least information associated with the fourth voltage.

14. The method of claim 13 wherein the first voltage is at the ground level.

15. The method of claim 13 wherein the processing information associated with the analog voltage and a fourth voltage is related to a successive approximation register.

16. The method of claim 15 wherein the adjusting the fourth voltage comprises:

adjusting each of the second plurality of capacitor terminals to one selected from a group consisting of the first voltage, the second voltage, and the third voltage in response to information associated with the analog voltage and the fourth voltage;

coupling the third voltage to one of the plurality of resistor terminals free from the second terminal in response to information associated with the analog voltage and the fourth voltage.

17. The method of claim 16 wherein the plurality of capacitors comprises 2^m capacitors, wherein m is an integer larger than zero.

18. The method of claim 17 wherein the coupling each of the second plurality of capacitor terminals comprises coupling 2^{m-1} capacitors to the second voltage and coupling the other 2^{m-1} capacitors to the first voltage.

19. The method of claim 18 wherein the processing information associated with the analog voltage and a fourth voltage and adjusting the fourth voltage comprises

if the fourth voltage is larger than the analog voltage, coupling 2^{m-2} capacitors to the second voltage and coupling the other 2^m-2^{m-2} capacitors to the first voltage, m being larger than 1.

20. The method of claim 19 wherein the processing information associated with the analog voltage and a fourth voltage and adjusting the fourth voltage comprises

if the fourth voltage is smaller than the analog voltage, coupling 2^{m-2} capacitors to the first voltage and coupling the other 2^m-2^{m-2} capacitors to the second voltage.